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EXAMINER	
SPITTLE, MATTHEW D	
ART UNIT	**PAPER NUMBER**
2111	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/759,232	CHUNG ET AL.	
	Examiner	Art Unit	
	Matthew D. Spittle	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 19-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 19-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 – 14, 19 – 34 have been examined.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 33 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 33 recites, "...a transfer unit..." Examiner is unable to find support in Applicant's disclosure for such a component.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 2, 5, 7, 8, 9, 12, and 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding claims 1, 2, 5, 7, 8, 9, 12 and 25, Examiner is unclear as to what data the "bit strings" refers to. Claim 1 recites, "...storing the bit strings configuring the read data in a DMA control register..."

Examiner interprets those bit strings as the bits that are stored in the DMA control register to configure the read data. Claim 12, as an example, recites, "...rearranges positions of less and more significant bit strings, and writes the read data to the second storage medium according to a result of the rearrangement." In this part of claim 12, the meaning of bit strings appears to refer to the manipulated read data. For this reason, Examiner finds the meaning of "the bit strings" in claims 1, 2, 5, 6, 8, 9, 12 and 25 to be ambiguous.

Claim Objections

Claims 25 and 27 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claims 25 and 27 both depend from claim 1, reciting substantially similar limitations as in claim 1, and thus fail to further limit.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1- 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tokumaru in view of Staplin et al.

With regard to claim 1, Tokumaru teaches a method for reading and storing data by means of a direct memory access (DMA) medium (Figure 4), comprising the steps of:

In the DMA medium (interpreted as a DMA controller), deciding a shift direction and a predetermined number of bits to be shifted in advance (column 3, line 64 – column 4, line 3; column 4, lines 18 – 22) when a request is made so that data read from a first storage medium (where a first storage medium may be interpreted as a first memory; column 3, lines 23 – 29) can be processed;

Shifting the bit strings by the predetermined number of bits in the decided shift direction, and transferring the shifted bit strings to a second storage medium (where a second storage medium may be interpreted as a destination memory; column 3, lines 23 – 29; column 2, lines 45 – 56).

Tokumaru fails to teach sequentially storing bit strings configuring the read data in a DMA control register.

Staplin et al. teach sequentially storing bit strings configuring the read data (specifically, the shift direction and number of shifts) in a register (interpreted as an F-register; Figure 3, item 51; column 9, lines 18 – 24; Table 1).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to store the shift configuring data as taught by Tokumaru into a register as taught by Staplin et al. This would have been obvious in order to store the configuration values, thereby making it unnecessary to re-compute them in the case where an identical operation is performed twice in a row, thus, making the DMA operation more efficient.

With regard to claim 2, Staplin et al. teach the additional limitation wherein each of the bit strings configuring the read data is configured by one of an 8-bit string, a 16-bit string, or a 32-bit string (column 12, lines 12 – 13).

With regard to claim 3, Staplin et al. teach the additional limitation wherein the number of bits to be shifted has a value from 0 to 7 (column 9, lines 50 – 55; Staplin et al. teach that 4 bits (bits 12 – 15) are used when bit 8 equals a binary 0 to determine the number of positions to be shifted. 4 bits would provide a range from 0 to 15).

With regard to claim 4, Tokumaru teaches the additional limitation wherein the step of deciding the shift direction and the number of bits to be shifted depends upon bit values set by the DMA medium (Examiner interprets the shifting signals, which determine the shift direction and number of bits (column 3, line 64 – column 4, line 3; column 4, lines 18 – 22) as being part of the DMA medium, and therefore the reference meets this limitation).

* * *

Examiner assumes that the applicant meant to recite classifying the read data, instead of classifying the bit strings configuring the read data in the following:

Claims 5 – 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tokumaru in view of Staplin et al., and further in view of Beukema et al.

With regard to claim 5, Tokumaru and Staplin et al. teach writing the bit strings configuring the read data to the second storage medium, but fail to teach classifying the bit strings configuring the read data into more significant bit strings and less significant bit strings; and rearranging positions of less and more significant bit strings.

Beukema et al. teach classifying bit strings into more significant bit strings and less significant bit strings and rearranging positions of less and more significant bit strings (Figure 6B, 7B, 8; where classifying bit strings and rearranging positions may be interpreted as reflection; column 9, lines 41 – 60; column 16, lines 60 – 67).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the method of Beukema into the method of Tokumaru and Staplin et al. This would have been obvious in order to provide DMA transfers on "mixed endian computing systems" in order to promote better performance when converting between the two types of data organization (column 2, lines 38 – 43; column 3, lines 51 – 56).

With regard to claim 6, Beukema et al. teach the additional limitation of wherein the bit strings configuring the read data is configured in the form of 32 bits at the step of rearranging the positions of the less and more significant bit strings (Figure 4C; column 5, lines 52).

With regard to claim 7, Beukema et al. teach the additional limitation of wherein the step of rearranging the positions of the less and more significant bit strings depends upon bit values set by the DMA medium (where a bit value may be interpreted as a "reflection bit" (RB); column 9, lines 41 – 58).

* * *

Claims 8 – 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tokumaru in view of Staplin et al.

With regard to claim 8, Tokumaru teaches an apparatus for reading and storing data by means of a director memory access (DMA) medium (Figure 4), comprising:

A first storage medium for storing data read in a source address (where a first storage medium may be interpreted as a first memory; column 3, lines 23 – 29) ;

The DMA medium for decoding a shift direction and a predetermined number of bits to be shifted in advance when a request is made so that the read data can be processed, sequentially storing bit strings configuring the read data, shifting the bit strings by the predetermined number of bits in the decided shift direction, and transferring the shifted bit strings (column 3, line 64 – column 4, line 3; column 4, lines 18 – 22);

A second storage medium for storing data transferred from the DMA medium (where a second storage medium may be interpreted as a destination memory; column 3, lines 23 – 29; column 2, lines 45 – 56).

Tokumaru fails to teach sequentially storing bit strings configuring the read data in a DMA control register.

Staplin et al. teach sequentially storing bit strings configuring the read data (specifically, the shift direction and number of shifts) in a register (interpreted as an F-register; Figure 3, item 51; column 9, lines 18 – 24; Table 1).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to store the shift configuring data as taught by Tokumaru into a register as taught by Staplin et al. This would have been obvious in order to store the configuration values, thereby making it unnecessary to re-compute them in the case

where an identical operation is performed twice in a row, thus, making the DMA operation more efficient.

With regard to claim 9, Staplin et al. teach the additional limitation wherein the DMA medium reads each of the bit strings configuring the data with one of an 8-bit string, a 16-bit string, or a 32-bit string (column 12, lines 12 – 13).

With regard to claim 10, Staplin et al. teach the additional limitation wherein the DMA medium carries out the shift operationg according to the number of bits to be shifted that has a value from 0 to 7 (column 9, lines 50 – 55; Staplin et al. teach that 4 bits (bits 12 – 15) are used when bit 8 equals a binary 0 to determine the number of positions to be shifted. 4 bits would provide a range from 0 to 15).

With regard to claim 11, Tokumaru teaches the additional limitation wherein the DMA medium decides the shift direction and the number of bits to be shifted depends upon bit values (Examiner interprets the shifting signals, which determine the shift direction and number of bits (column 3, line 64 – column 4, line 3; column 4, lines 18 – 22) as being part of the DMA medium, and therefore the reference meets this limitation).

* * *

Examiner assumes that the applicant meant to recite classifying the read data, instead of classifying the bit strings configuring the read data in the following:

Claim 12 – 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tokumaru in view of Staplin et al., and further in view of Beukema et al.

With regard to claim 12, Tokumaru and Staplin et al. teach writing the bit strings configuring the read data to the second storage medium, but fail to teach the DMA medium classifying the bit strings configuring the read data into more significant bit strings and less significant bit strings; and rearranging positions of less and more significant bit strings.

Beukema et al. teach the DMA medium classifying bit strings into more significant bit strings and less significant bit strings and rearranging positions of less and more significant bit strings (Figure 6B, 7B, 8; where classifying bit strings and rearranging positions may be interpreted as reflection; column 9, lines 41 – 60; column 16, lines 60 – 67).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the method of Beukema into the method of Tokumaru and Staplin et al. This would have been obvious in order to provide DMA transfers on "mixed endian computing systems" in order to promote better performance when converting between the two types of data organization (column 2, lines 38 – 43; column 3, lines 51 – 56).

With regard to claim 13, Beukema et al. teach the additional limitation of wherein the DMA medium rearranges the positions of the less and more significant bit strings when the bit strings configuring the read data is configured in the form of 32 bits (Figure 4C; column 5, lines 52).

With regard to claim 14, Beukema et al. teach the additional limitation of wherein the DMA medium rearranges the positions of the less and more significant bit strings depends upon bit values (where a bit value may be interpreted as a "reflection bit" (RB); column 9, lines 41 – 58).

* * *

Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tokumaru in view of Staplin et al. and Black (OSI – A Model for Computer Communications Standards).

Regarding claim 19, Tokumaru and Staplin et al. fail to explicitly teach the limitations including first and second layers, however, Examiner notes that both Tokumaru and Staplin et al. are geared toward improving communication between computer systems and components.

Black provides a set of standards that allow for compatible communications between varying types of computer systems and hardware, including:

At a second layer, receiving at least one first layer data packet from a first layer and storing said at least one first layer data packet in the first storage medium which corresponds to the second layer by shifting said at least one first layer data packet by as many bits as indicated by a second layer header (p. 7 – 9; p. 31, Fig. 1-14);

Adding the second layer header infront of said at least one first layer data packet to make a second layer data packet (as shown on p. 7, Fig. 1-2);

Transferring at least one second layer data packet to a third layer (p. 9, Fig. 1-3),

Wherein said second layer header includes control information for said second layer data packet (p. 33, par. 1 – 3).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate the OSI model as taught by Black into the computer communication systems of Tokuarmu and Staplin et al. for the purpose of providing a standardized means of communication between multiple systems. This would have been obvious in order to make the systems compatible with one another, thereby offering more flexibility to the user in terms of software and hardware selection.

Regarding claim 20, Black teaches the additional limitation comprising:

At said third layer, receiving said at least one second layer data packet and storing said at least one second layer data packet in the second storage medium whicih corresponds to the third layer (p. 9, Fig. 1-3);

Adding cyclic redundancy checking (CRC) at the rear of said at least one second layer data packet to make a third layer data packet (p. 32 – 33, 114 – 115, 285).

Regarding claim 24, Tokumaru teaches the additional limitation wherein the transfer between the layers is performed by direct memory access (DMA) (ABSTRACT).

Regarding claims 25 and 27, Tokumaru teaches the additional limitation of deciding a shift direction and a predetermined number of bits to be shifted in advance (column 3, line 64 – column 4, line 3; column 4, lines 18 – 22) when a request is made so that data read from a first storage medium (where a first storage medium may be interpreted as a first memory; column 3, lines 23 – 29) can be processed;

Shifting the bit strings by the predetermined number of bits in the decided shift direction, and transferring the shifted bit strings to a second storage medium (where a second storage medium may be interpreted as a destination memory; column 3, lines 23 – 29; column 2, lines 45 – 56).

Tokumaru fails to teach sequentially storing bit strings configuring the read data in a DMA control register.

Staplin et al. teach the additional limitation of sequentially storing bit strings configuring the read data (specifically, the shift direction and number of shifts) in a register (interpreted as an F-register; Figure 3, item 51; column 9, lines 18 – 24; Table 1).

Regarding claim 26, Black teaches the additional limitation wherein the shift direction and size of bits to be shifted is decided according to information in a header (p.

31, Fig. 1-14 shows how the packet bits are shifted when the header is added to the packet as it travels between layers. Thus Black inherently teaches the limitation of shifting and shift direction.).

* * *

Claims 21 – 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tokumaru in view of Staplin et al. and Black (OSI – A Model for Computer Communications Standards) and what is old and well known in this art as evidenced by Lundsjo et al. (U.S. 6,473,442), Chuah et al. (U.S. 6,400,695), Hamalainen et al. (U.S. 6,359,904) and Yi et al. (U.S. 7,054,270).

Regarding claims 21 – 23, Black teaches wherein the third layer comprises a physical (PHY) layer (p. 9, Fig 1-3), but fails to explicitly teach wherein the first layer is a radio link control (RLC) layer and the second layer is a medium access control (MAC) layer.

Examiner takes official notice that a protocol stack of this type is old and well known in this art. This is evidenced by Lundsjo et al. (Fig. 2), Chuah et al. (Fig. 2), Hamalainen et al. (Fig. 2a), and Yi et al. (Fig. 1).

* * *

Claims 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tokumaru in view of Staplin et al. and Black (OSI – A Model for Computer Communications Standards).

Regarding claim 28, Tokumaru and Staplin et al. fail to explicitly teach the limitations including first and second layers, however, Examiner notes that both Tokumaru and Staplin et al. are geared toward improving communication between computer systems and components.

Black provides a set of standards that allow for compatible communications between varying types of computer systems and hardware, including:

Wherein a data packet is generated in a mobile communication system (interpreted as a computeR) and data is shifted by means of a protocol layer (as shown on p. 31, Fig. 1-14) , and the DMA operates to transfer at least one first layer data packet form a first layer to a second layer, said second layer to receive said at least one first layer data packet from a first layer, to store said at least one first layer data packet in the first storage medium which corresponds to the second layer by shifting said at least one first layer data packet by as many bits as indicated by a second layer header, to add the second layer header in front of said at least one first layer data packet ot make a second layer data packet and to transfer at least one second layer data packet to a third layer, said second layer header comprising control information for said second layer data packet (p. 7 – 9; Fig 1-2; Fig. 1-3; p. 33, par. 1 – 3).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate the OSI model as taught by Black into the

computer communication systems of Tokuarmu and Staplin et al. for the purpose of providing a standardized means of communication between multiple systems. This would have been obvious in order to make the systems compatible with one another, thereby offering more flexibility to the user in terms of software and hardware selection.

Regarding claim 29, Black teaches the additional limitation comprising:

At said third layer, receiving said at least one second layer data packet and storing said at least one second layer data packet in the second storage medium whicih corresponds to the third layer (p. 9, Fig. 1-3);

Adding cyclic redundancy checking (CRC) at the rear of said at least one second layer data packet to make a third layer data packet (p. 32 – 33, 114 – 115, 285).

* * *

Claims 30 – 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tokumaru in view of Staplin et al. and Black (OSI – A Model for Computer Communications Standards) and what is old and well known in this art as evidenced by Lundsjo et al. (U.S. 6,473,442), Chuah et al. (U.S. 6,400,695), Hamalainen et al. (U.S. 6,359,904) and Yi et al. (U.S. 7,054,270).

Regarding claims 30 – 32, Black teaches wherein the third layer comprises a physical (PHY) layer (p. 9, Fig 1-3), but fails to explicitly teach wherein the first layer is a

radio link control (RLC) layer and the second layer is a medium access control (MAC) layer.

Examiner takes official notice that a protocol stack of this type is old and well known in this art. This is evidenced by Lundsjo et al. (Fig. 2), Chuah et al. (Fig. 2), Hamalainen et al. (Fig. 2a), and Yi et al. (Fig. 1).

Claim 34 recites limitations substantially similar as in claims 1 and 19 – 27, and is therefore rejected under the same grounds.

Response to Arguments

Applicant's arguments filed 12/22/2006 have been fully considered but they are not persuasive.

Regarding Applicant's argument that Tokumaru fails to teach deciding a shift direction within the DMA medium, Examiner points to col. 7, lines 56 – 63 which disclose that all data transfer operations, including the required shifting and selecting as described through the remainder of column 7, are carried out in the DMA controller.

Regarding Applicant's argument that Staplin teaches away from the claimed invention, Examiner notes that the Staplin reference is used to show that control information for data shifting can be stored in a register, irrespective of whether it's in a processor or DMA controller. The purpose of storing this control information in a register is to allow for a variation in the timing as to when the data shifting operation (or

any other operation) could be performed. For example, the control information could be stored in the register at time t=0 and then used later at some time t > 0. Without using a register, it becomes necessary for the control information to be utilized at the same instant it becomes available. Another reason to use a register is to allow for more efficient repeat-operations. By storing the control information and repeatedly using it, a processing element need only generate it a single time. Staplin does not teach that their register should not be used in a DMA controller. Staplin is not cited for describing data shifting.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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